EVB-LAN8187

LAN8187(I) MII Customer Evaluation Board

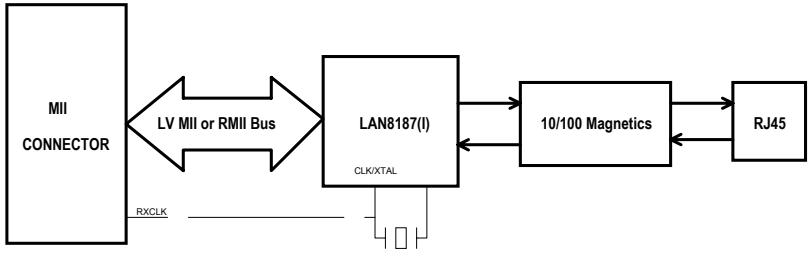
Schematic Revision B

Design Details

Board: PCB-7058AZ-B
Chip: LAN8187I
Board Form Factor:
Assembly:

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

EVB BLOCK DIAGRAM



Default: MII mode RXCLK Not connected to CLK/XTAL
RMII mode XTAL removed and RXCLK Is connected to CLK/XTAL

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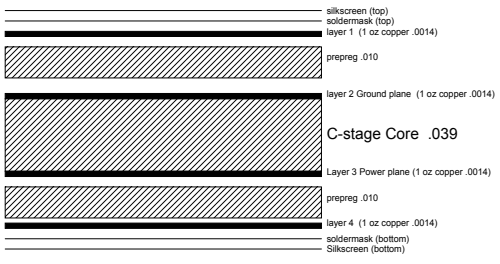
Revisions
Rev A001 added 15pF caps to outputs
Rev A002 swapped vddio and vdd33 power pins; corrected mdio pullup voltage; clarified mode table
Rev A003 corrected all other vddio pullups.
Rev A004 changed all (i) to (I)
Rev A005 deleted extra caps on 5V power supply; added FB6 to pin 1 of MII for VDDIO power; added note to move R54 close to R13; remove C6 and C21; add note to keep C15 and C16 close to reg; and added config option for MII pin 22 to be either gnd or nRST; added config option for MII pin 21 to be either gnd or gpo

Rev B added POE access header and changed power net name on pin 13 of PHY to VDD from VDD33

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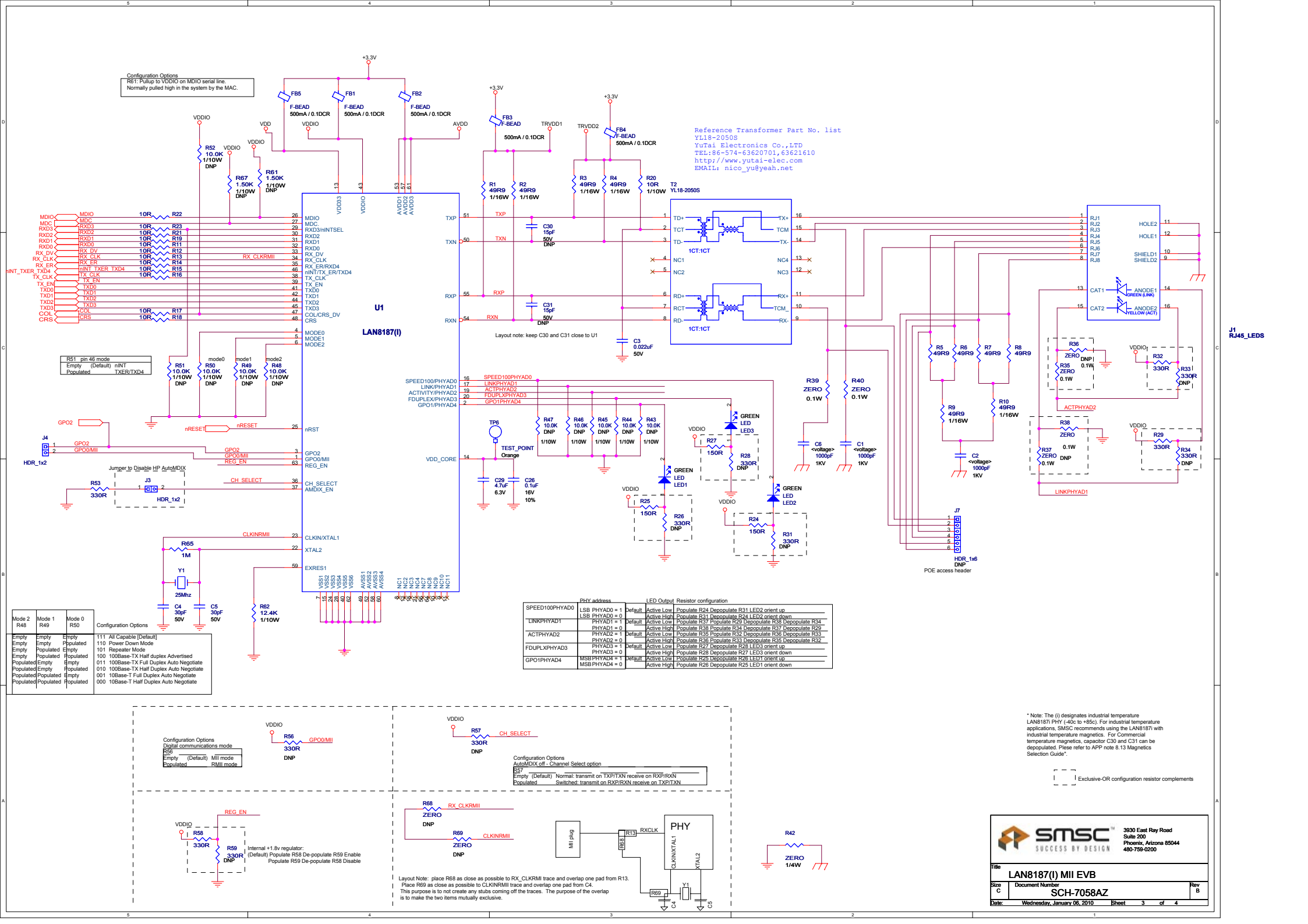
stackup



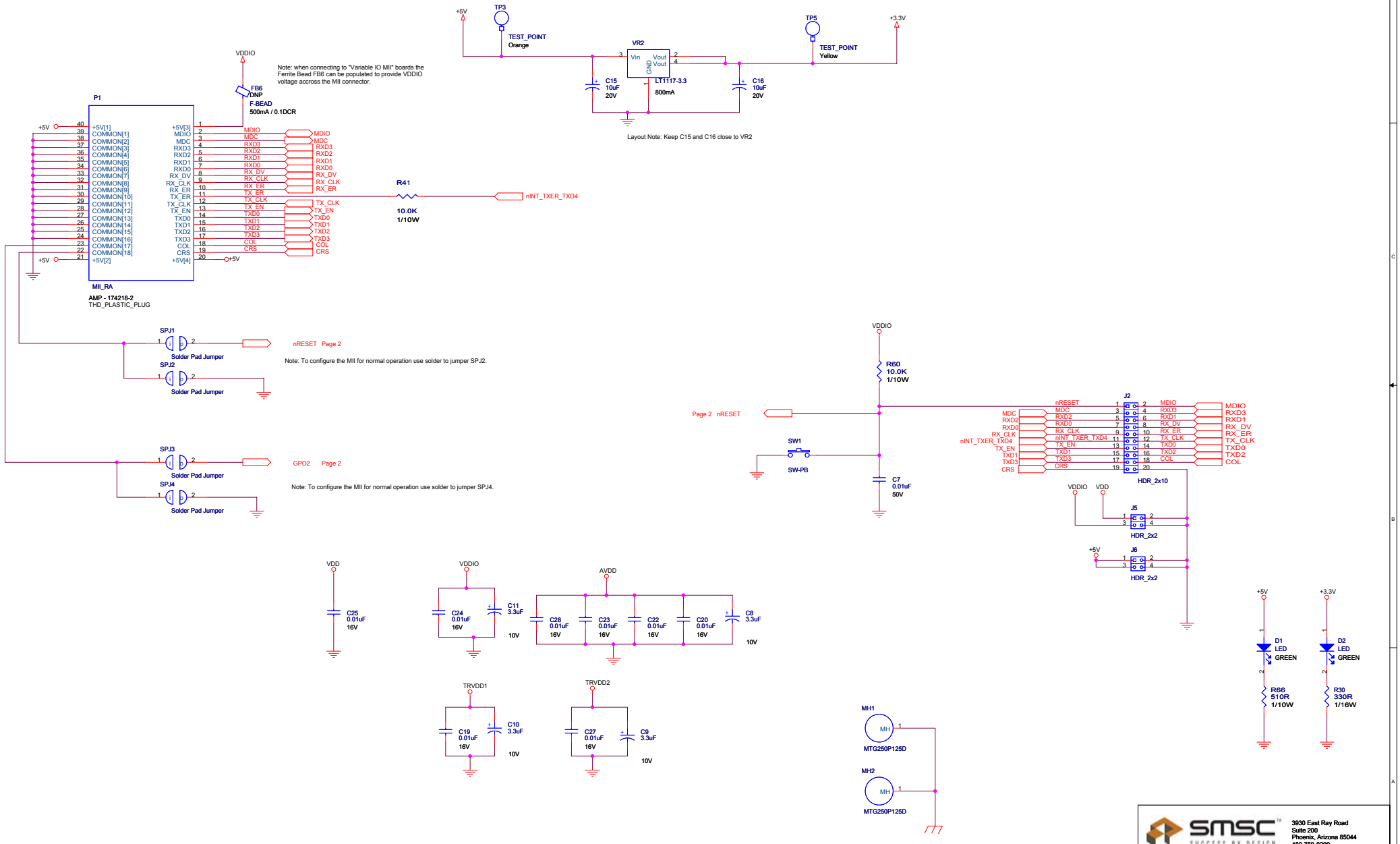
NOTES:
1. BOARD FABRICATION AND QUALITY ACCEPTANCE PER IPC-6012 CLASS 2. BOARD MUST MEET OR EXCEED QUALIFICATION TESTING AND QUALITY CONFORMACE TESTING INSPECTION SPECIFIED WITHIN.
2. MATERIAL: NEMA GRADE STANDARD FR4. LAMINATED SHEET, HTE 1 OZ COPPER CLAD, TYPE GF/GFG WOVEN GLASS BASE, FLAME RESISTANCE MEETING UL94V-0 OR BETTER. MATERIAL IN ACCORDANCE WITH IPC-4101.
3. BOARD FABRICATION SHALL APPLY DATE CODE, FABRICATOR'S CAGE CODE, I.D. AND UL MARKING TO SECONDARY SIDE WHERE INDICATED. MARKING PREFERABLY COPPER ETCHED. EPOXY INK ACCEPTABLE.
4. SOLDERMASK,USING TYPEB,PHOTO IMAGEABLE LPI FILM 0.0015 THICK. APPLY TO BOTH SIDES IN ACCORDANCE WITH IPC-SM-840 (TYPE B CLASS 3). USE APPROPIATE SOLDER MASK ARTWORK FOR EACH SIDE. PUNCTURING OF PUNCTURING OF TENTED HOLES IS PERMISSIBLE. SOLDERMASK MISREGISTRATION SHALL NOT EXCEED .004 INCH. SOLDERMASK OVERLAP PERMITTED ON CIRCULAR LANDS ONLY AND SHALL NOT EXCEED 0.001 INCH. NO OVERLAP PERMITTED ON RECTANGULAR LANDS.
5. FINISH: SOLDER MASK OVER BARE COPPER (SMOBC), HOT AIR LEVEL DEPOSIT
6. DRILL BOARDS USING DRILL DATA, DRILL PATTERN AND HOLE SCHEDULE. HOLE LOCATION MAY VARY WITHIN .004 IN. MAX ABOUT TRUE POSITION.
7. MINIMUM ANNULAR RINGS:
   .002 IN MINIMUM - EXTERNAL LAYERS.
   .001 IN MINIMUM - INTERNAL LAYERS.
8. ALL EXPOSED SURFACE LANDS AND LINES TO BE SOLDER COATED.
9. ALL HOLES ARE PLATED THROUGH UNLESS NOTED OTHERWISE. MINIMUM COPPER PLATING IN PLATED HOLES TO BE .001 IN. COPPER PLATING IN TENTED HOLES SHALL NOT PLUG HOLES WITHOUT PERMISSION FROM SMSC.
10. COMPONENT MARKINGS: SILKSCREEN BOTH SIDES USING NON-CONDUCTIVE WHITE EPOXY INK. LANDS AND EXPOSED PLATED AREAS TO BE FREE OF INK.
11. DIMENSIONS ARE AFTER ETCHING AND PLATING AND ARE BASIC UNLESS OTHERWISE INDICATED.
12. BARE BOARD ELECTRICAL TEST: BARE BOARDS SHALL BE ELECTRICALLY TESTED USING CAD GENERATED NET LIST DATA. THIS INFORMATION TO BE SUPPLIED IN IPC-D-356 FORMAT. ELECTRICAL TESTING SHALL FOLLOW THE GUIDELINES EXTABLISHED BY IPC-ET-652. GUIDELINES AND REQUIREMENTS FOR ELECTRICAL TESTING OF PRINTED WIRING BOARDS.

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Configuration Options
R61: Pullup to VDDIO on MDIO serial line.
Normally pulled high in the system by the MAC.
Reference Transformer Part No. list
YL18-2050S
YuTai Electronics Co.,LTD
TEL:86-574-63620701,63621610
http://www.yutai-elec.com
EMAIL: nico_yu@yeah.net
U1
LAN8187(I)
T2
YL18-2050S
J1
RJ45_LEDS
Layout note: keep C30 and C31 close to U1
R51_pin 46 mode
Empty (Default) nINT
Populated TXER/TXD4
Jumper to Disable HP AutoMDIX
HDR_1x2
TEST_POINT
Orange
GREEN LED LED1
GREEN LED LED2
GREEN LED LED3
HDR_1x6
DNP
POE access header
Mode 2 R48 | Mode 1 R49 | Mode 0 R50 | Configuration Options
Empty | Empty | Empty | 111 All Capable [Default]
Empty | Empty | Populated | 110 Power Down Mode
Empty | Populated | Empty | 101 Repeater Mode
Empty | Populated | Populated | 100 100Base-TX Half duplex Advertised
Populated | Empty | Empty | 011 100Base-TX Full Duplex Auto Negotiate
Populated | Empty | Populated | 010 100Base-TX Half Duplex Auto Negotiate
Populated | Populated | Empty | 001 10Base-T Full Duplex Auto Negotiate
Populated | Populated | Populated | 000 10Base-T Half Duplex Auto Negotiate
SPEED100PHYAD0 | PHY address LSB PHYAD0 = 1 | Default | LED Output Active Low | Resistor configuration Populate R24 Depopulate R31 LED2 orient up
LSB PHYAD0 = 0 | Active High | Populate R31 Depopulate R24 LED2 orient down
LINKPHYAD1 | PHYAD1 = 1 | Default | Active Low | Populate R37 Depopulate R29 Depopulate R38 Depopulate R34
PHYAD1 = 0 | Active High | Populate R38 Depopulate R34 Depopulate R37 Depopulate R29
ACTPHYAD2 | PHYAD2 = 1 | Default | Active Low | Populate R36 Depopulate R32 Depopulate R36 Depopulate R33
PHYAD2 = 0 | Active High | Populate R36 Depopulate R33 Depopulate R35 Depopulate R32
FDUPLXPHYAD3 | PHYAD3 = 1 | Default | Active Low | Populate R27 Depopulate R28 LED3 orient up
PHYAD3 = 0 | Active High | Populate R28 Depopulate R27 LED3 orient down
GPO1PHYAD4 | MSB PHYAD4 = 1 | Default | Active Low | Populate R25 Depopulate R26 LED1 orient up
MSB PHYAD4 = 0 | Active High | Populate R26 Depopulate R25 LED1 orient down
Configuration Options
Digital communications mode
R56
Empty (Default) MII mode
Populated RMII mode
Configuration Options
AutoMDIX off - Channel Select option
R57
Empty (Default) Normal: transmit on TXP/TXN receive on RXP/RXN
Populated Switched: transmit on RXP/RXN receive on TXP/TXN
Internal +1.8v regulator:
(Default) Populate R58 De-populate R59 Enable
Populate R59 De-populate R58 Disable
Layout Note: place R68 as close as possible to RX_CLKRMII trace and overlap one pad from R13. Place R69 as close as possible to CLKINRMII trace and overlap one pad from C4. This purpose is to not create any stubs coming off the traces. The purpose of the overlap is to make the two items mutually exclusive.
MII plug
PHY
* Note: The (i) designates industrial temperature LAN8187i PHY (-40c to +85c). For industrial temperature applications, SMSC recommends using the LAN8187i with industrial temperature magnetics. For Commercial temperature magnetics, capacitor C30 and C31 can be depopulated. Please refer to APP note 8.13 Magnetics Selection Guide".
Exclusive-OR configuration resistor complements
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+5V MII to +3.3V Regulator



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