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KS8995M Integrated 5-Port 10/100 Managed Switch

Overview

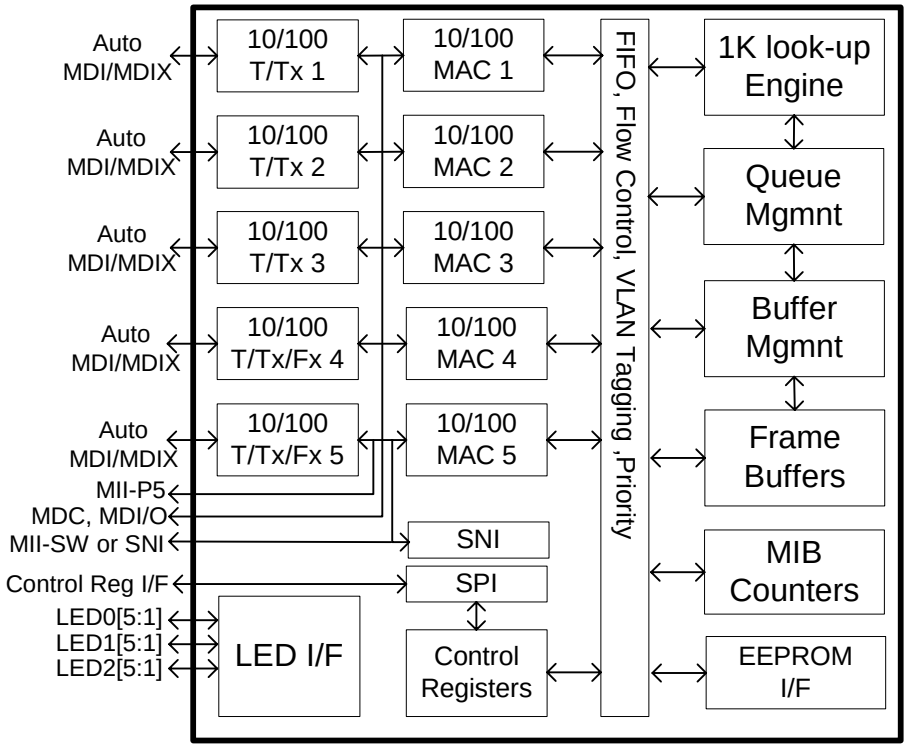
The KS8995M is a highly integrated layer-2 managed switch with optimized BOM (Bill-Of-Materials) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set such as tag/port-based VLAN, QoS priority, management, MIB counters, dual MII interface and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KS8995M contains five 10/100 transceivers with patented mixed-signal low-power technology, five MAC (Media Access Control) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10Base-T and 100Base-Tx. In addition, two of the PHY units support 100Base-Fx (Ports 4 & 5).

Feature Highlights

- Integrated switch with 5 MACs and 5 Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully non-blocking configuration
- 1.4Gbps high performance memory bandwidth
- 10Base-T, 100Base-TX and 100Base-FX modes (Fx in Ports 4 & 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)



KS8995M

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Feature Highlights (Cont'd)

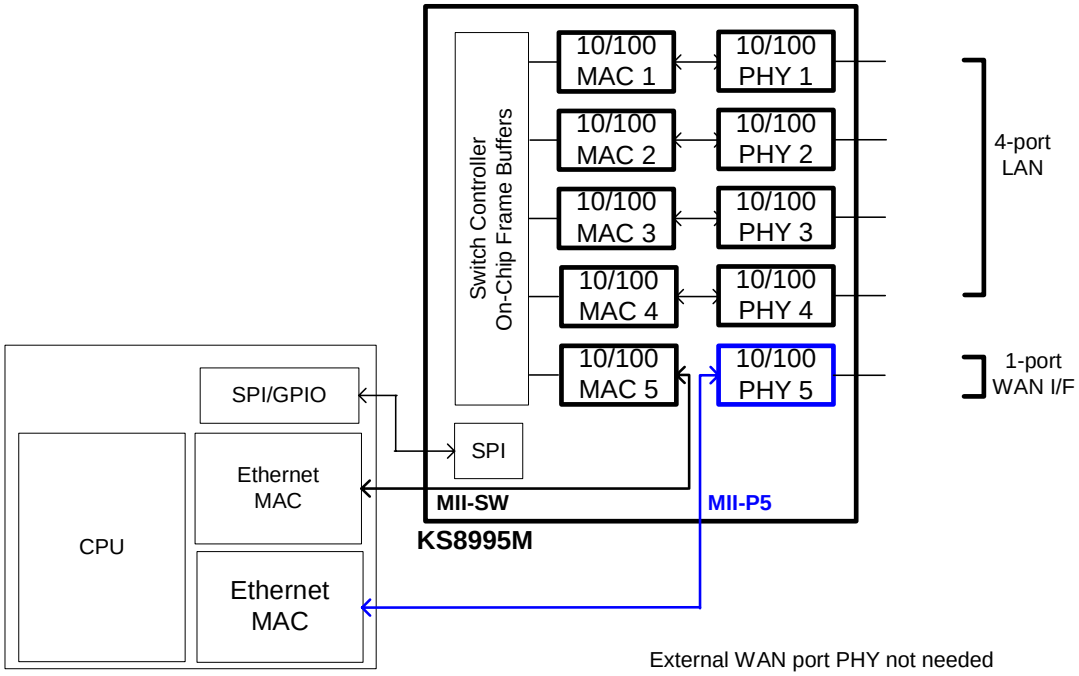
- IEEE 802.1Q tag-based VLAN (16 VLANs, full-range VID) for DMZ port, WAN/LAN separation or inter-VLAN switch links
- VLAN ID tag/untag options, per-port basis
- Programmable rate limiting 0 to 100Mbps, ingress & egress port, rate options for high & low priority, per port basis
- Flow control or drop packet rate limiting (ingress port)
- Integrated MIB counters for fully compliant statistics gathering, 34 MIB counters per port
- Enable/Disable option for huge frame size up to 1916 bytes per frame
- IGMP v1/v2 Snooping for multicast packet filtering
- Special tagging mode to send CPU info on ingress packet's port value
- SPI slave (complete) and MDIO (MII PHY only) serial management interface for control of register configuration
- MAC-id based security lock option
- Control registers configurable on-the-fly (port-priority, 802.1P/D/Q, AN…)
- CPU read access to MAC forwarding table entries
- 802.1D Spanning Tree Protocol
- Port mirroring / monitoring / sniffing: ingress and/or egress traffic to any port or MII
- Broadcast storm protection with % control - global & per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)
- QoS / CoS packets prioritization supports: per port, 802.1P and DiffServ based.
- 802.1p/q tag insertion or removal on a per port basis (egress)
- MDC & MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- Wire speed reception and transmission
- Integrated look-up engine with dedicated 1 K MAC addresses
- Full duplex IEEE 802.3x & half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI / MDI-X crossover for plug-and-play
- Low power, 1.8/2.5/3.3V, 0.18um CMOS technology
- 128 pin PQFP package

Applications

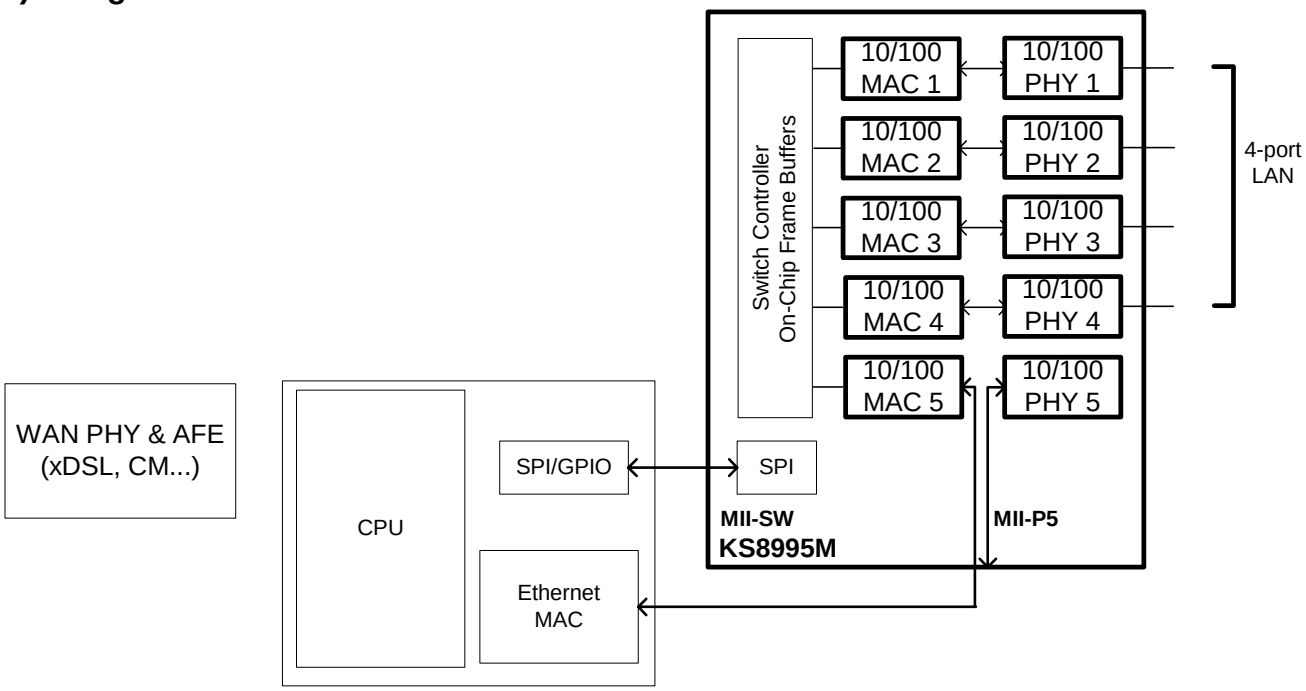
- Broadband gateway / firewall / VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point + gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel / Campus / MxU gateway
- Enterprise VoIP Gateway / Phone
- FTTx customer premise equipment
- Managed Media converter

System Level Configurations:

1) Broadband Gateway



2) Integrated Broadband Router



3) Standalone switch