

# SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDAS214E – DECEMBER 1982 – REVISED AUGUST 2002

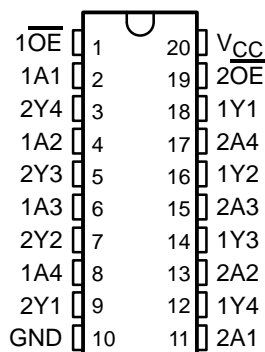
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading

SN54ALS240A, SN54AS240A . . . J OR W PACKAGE  
SN74ALS240A . . . DB, DW, N, OR NS PACKAGE  
SN74AS240A . . . DW OR N PACKAGE  
(TOP VIEW)

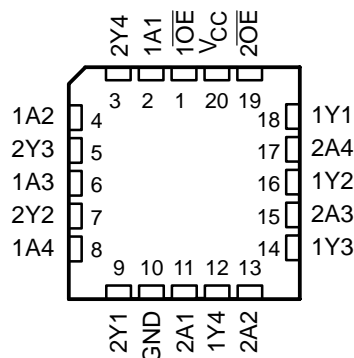
## description/ordering information

These octal buffers/drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. When these devices are used with the 'ALS241, 'AS241A, 'ALS244, and 'AS244A devices, the circuit designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

The -1 version of SN74ALS240A is identical to the standard version, except that the recommended maximum  $I_{OL}$  for the -1 version is 48 mA. There is no -1 version of the SN54ALS240A.



SN54ALS240A, SN54AS240A . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS240AN	SN74ALS240AN
			SN74ALS240A-1N	SN74ALS240A-1N
			SN74AS240AN	SN74AS240AN
	SOIC – DW	Tube	SN74ALS240ADW	ALS240A
			SN74ALS240ADWR	
		Tape and reel	SN74ALS240A-1DW	ALS240A-1
			SN74ALS240A-1DWR	
		Tube	SN74AS240ADW	AS240A
			SN74AS240ADWR	
	SOP – NS	Tape and reel	SN74ALS240ANSR	ALS240A
			SN74ALS240A-1NSR	ALS240A-1
	SSOP – DB	Tape and reel	SN74ALS240ADBR	G240A
			SN74ALS240A-1DBR	G240A-1

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A**  
**OCTAL BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**description/ordering information (continued)**

**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – J	Tube	SNJ54ALS240AJ	SNJ54ALS240AJ
			SNJ54AS240AJ	SNJ54AS240AJ
	CFP – W	Tube	SNJ54ALS240AW	SNJ54ALS240AW
			SNJ54AS240AW	SNJ54AS240AW
	LCCC – FK	Tube	SNJ54ALS240AFK	SNJ54ALS240AFK
			SNJ54AS240AFK	SNJ54AS240AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**  
**(each buffer)**

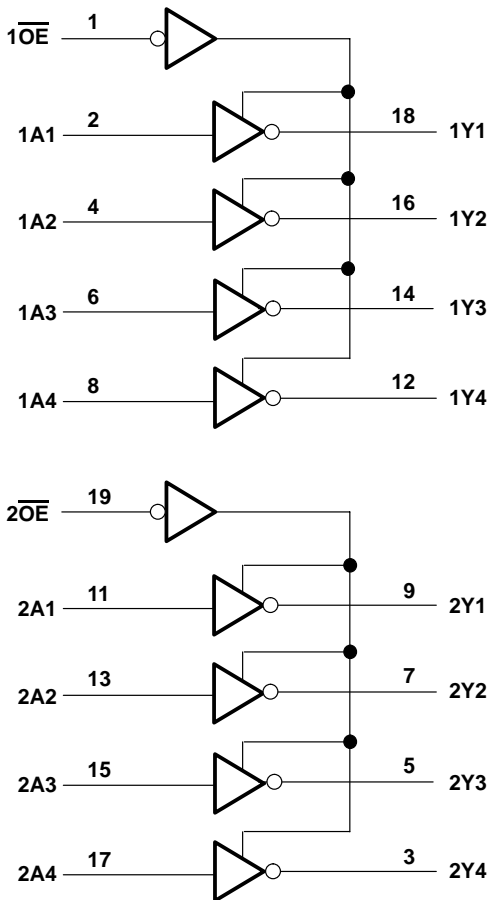
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z



# SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1):	
DB package	70°C/W
DW package	58°C/W
N package	70°C/W
NS package	60°C/W
Storage temperature range, $T_{Stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage	SN54ALS240A		0.7	V
		SN74ALS240A, 'AS240A		0.8	
I <sub>OH</sub>	High-level output current	SN54ALS240A, SN54AS240A		-12	mA
		SN74ALS240A, SN74AS240A		-15	
I <sub>OL</sub>	Low-level output current	SN54ALS240A		12	mA
		SN74ALS240A		24	
				48†	
				64	
T <sub>A</sub>	Operating free-air temperature	SN54ALS240A, SN54AS240A		-55	°C
		SN74ALS240A, SN74AS240A		0	

† Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS240A		SN74ALS240A		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		V		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> - 2		V <sub>CC</sub> - 2		V		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.2	2.4		3.2	
		I <sub>OH</sub> = -12 mA	2					
		I <sub>OH</sub> = -15 mA			2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V	
		I <sub>OL</sub> = 24 mA			0.35	0.5		
		I <sub>OL</sub> = 48 mA†			0.35	0.5		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			20		μA		
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V			-20		μA		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1		mA		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20		μA		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V			-0.1		mA		
I <sub>O§</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-20		-112	-30	-112	mA	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	Outputs high		4	11	4	11	mA
		Outputs low		13	23	13	23	
		Outputs disabled		14	25	14	25	

† Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>.



# SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS240A		SN74AS240A		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$	-1.2		-1.2		V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	$I_{OH} = -2\text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$		V
		$I_{OH} = -3\text{ mA}$	2.4	3.4	2.4	3.4	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -12\text{ mA}$	2.4				
		$I_{OH} = -15\text{ mA}$			2.4		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.27	0.55			V
		$I_{OL} = 64\text{ mA}$			0.31	0.55	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$	50		50		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$	-50		-50		$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$	0.1		0.1		mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$	20		20		$\mu\text{A}$
$I_{IL}$	A inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		-1		mA
	$\overline{OE}$ inputs				-0.5		
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-50	-150	-50	-150	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	11	17	11	17	mA
		Outputs low	51	75	51	75	
		Outputs disabled	24	38	24	38	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$				UNIT
			SN54ALS240A		SN74ALS240A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	2	22	2	9	ns
$t_{PHL}$			2	11	2	9	
$t_{PZH}$	$\overline{OE}$	Y	4	34	5	13	ns
$t_{PZL}$			5	26	5	18	
$t_{PHZ}$	$\overline{OE}$	Y	1	15	2	10	ns
$t_{PLZ}$			3	24	3	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A**  
**OCTAL BUFFERS/DRIVERS**  
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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS240A		SN74AS240A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1	7	1	6.5	ns
t <sub>PHL</sub>			1.2	6.5	1.2	6.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	1	7	1	6.4	ns
t <sub>PZL</sub>			1.1	9.5	1.1	9	
t <sub>PHZ</sub>	$\overline{OE}$	Y	1.2	5.5	1.2	5	ns
t <sub>PLZ</sub>			1.5	12.5	1.5	9.5	

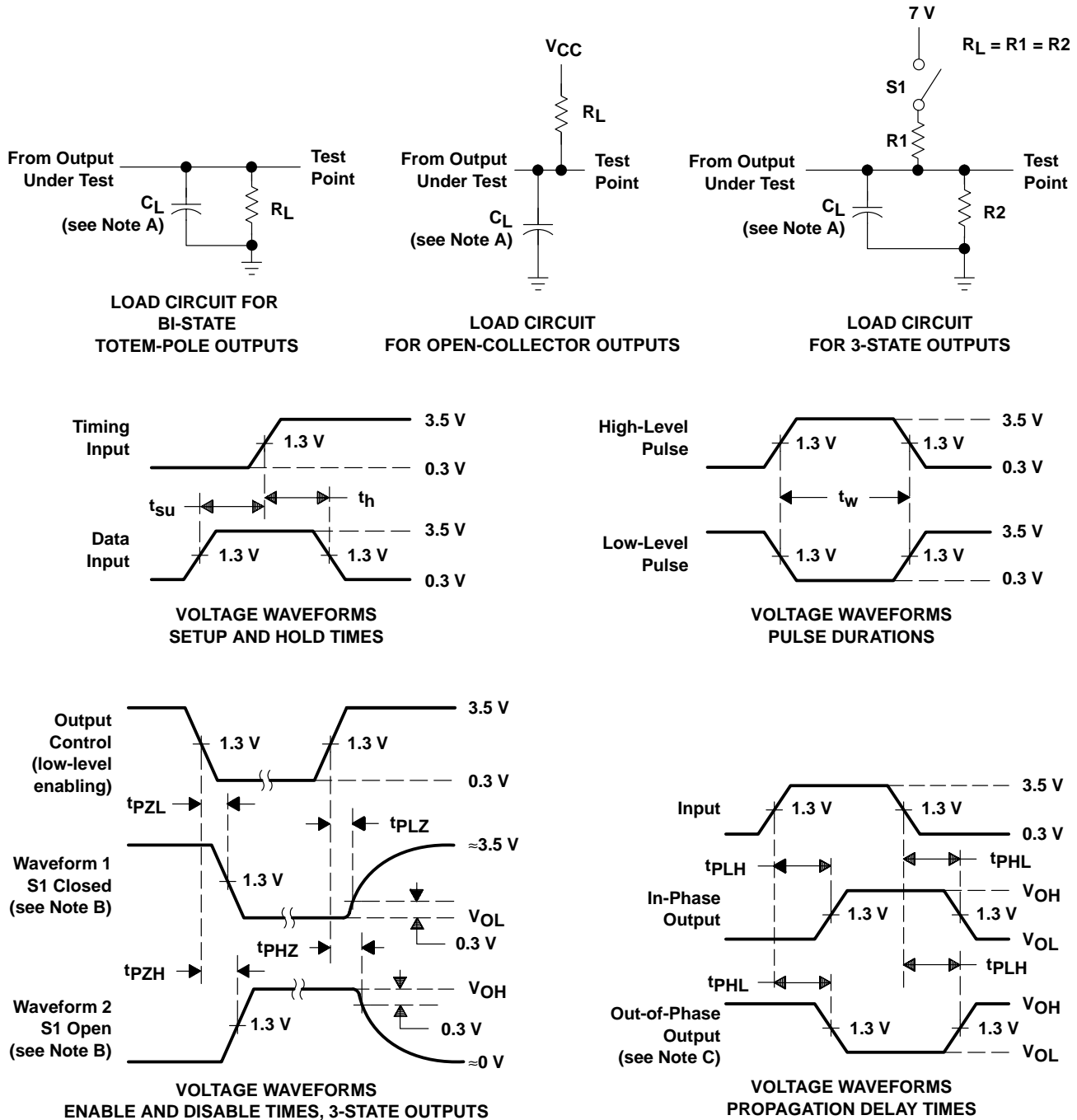
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8859101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/38301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/38301BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN54ALS240AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN54AS240AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN74ALS240A-1DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS240A-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS240A-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240A-1NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS240ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS240ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS240ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS240ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS240ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS240ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS240AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS240AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54ALS240AW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54AS240AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS240AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS240AW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

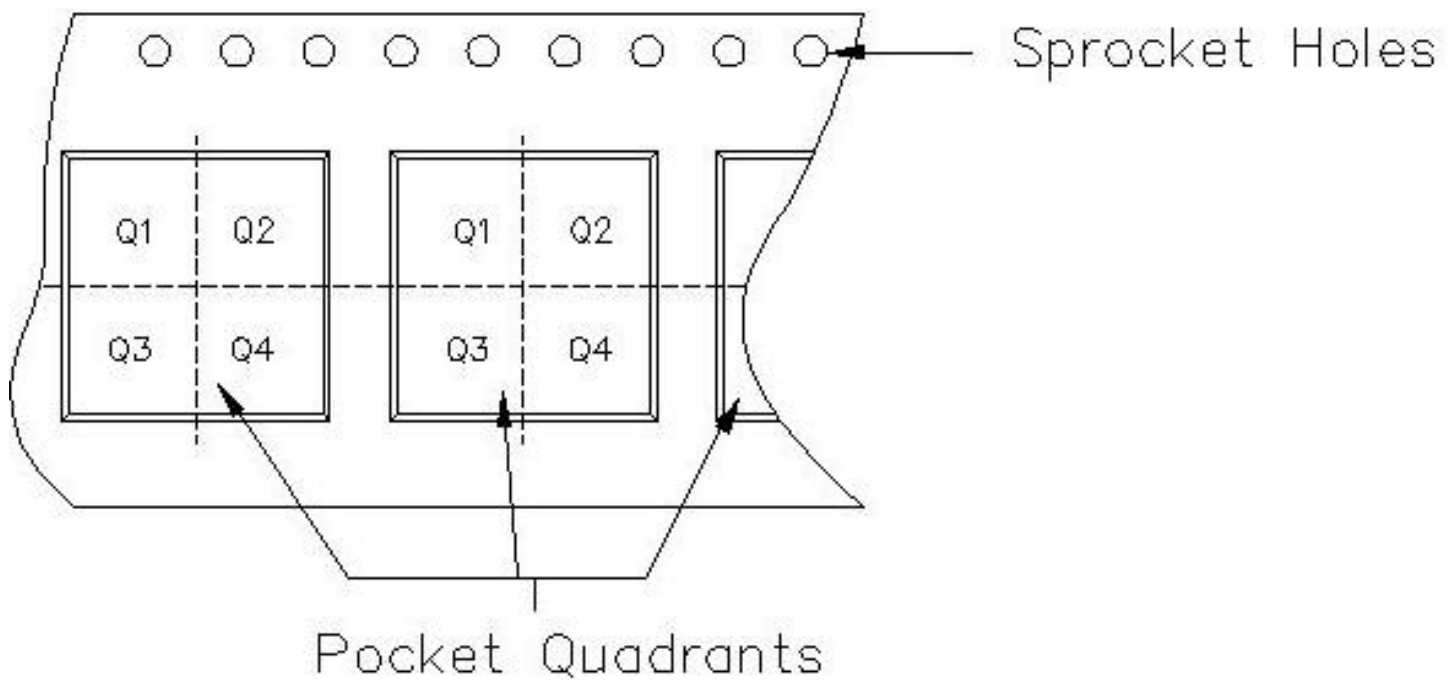
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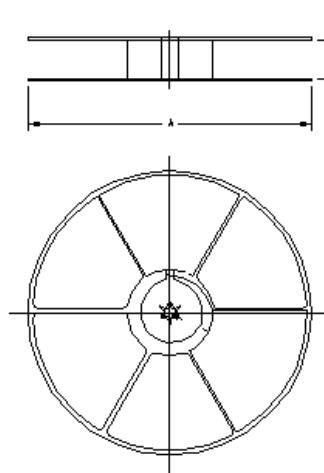
Carrier tape design is defined largely by the component length, width, and thickness.

$Ao$ = Dimension designed to accommodate the component width.
$Bo$ = Dimension designed to accommodate the component length.
$Ko$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



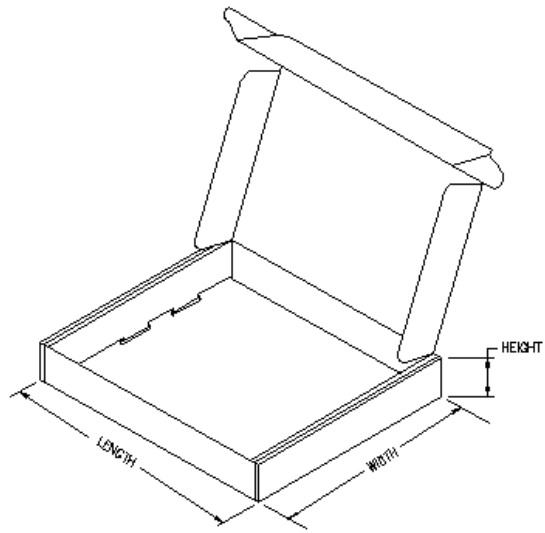
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS240A-1DBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74ALS240A-1DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74ALS240A-1NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74ALS240ADWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74ALS240ANSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74AS240ADWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74AS240ANSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALS240A-1DBR	DB	20	MLA	346.0	346.0	33.0
SN74ALS240A-1DWR	DW	20	MLA	333.2	333.2	31.75
SN74ALS240A-1NSR	NS	20	MLA	333.2	333.2	31.75
SN74ALS240ADWR	DW	20	MLA	333.2	333.2	31.75
SN74ALS240ANSR	NS	20	MLA	333.2	333.2	31.75
SN74AS240ADWR	DW	20	MLA	333.2	333.2	31.75
SN74AS240ANSR	NS	20	MLA	333.2	333.2	31.75



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

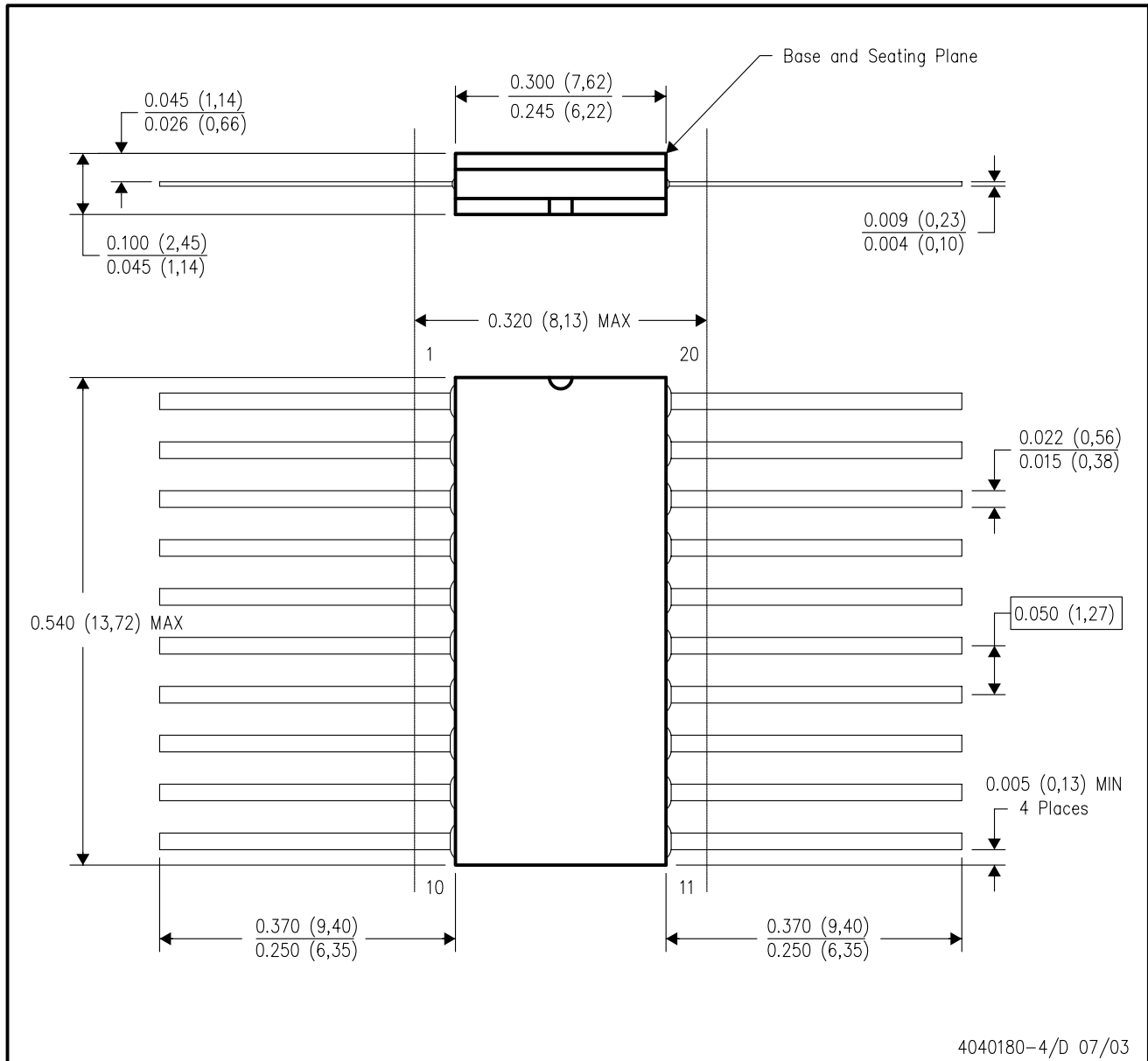


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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